REMARKS

The Office Action dated January 26, 2005 has been carefully considered. Claims 1-17 are pending. The above amendments and the following remarks are presented in a sincere attempt to place this Application in condition for allowance. Claims 1-3 and 5-9 have been amended, and Claims 10-17 have been added in this Response. Reconsideration and allowance are respectfully requested in light of the above amendments and following remarks.

An interview was held with the Examiner, Mr. An T. Luu, on March 22, 2005, to discuss the rejections under 35 U.S.C. § 103(a) and the proposed amendments thereto. Applicants wish to thank the Examiner for his time and the courtesies extended.

Claims 1-6 stand rejected under 35 U.S.C. § 102(b) in view of U.S. Patent 5,781,048 to Nakao et al. ("Nakao"). Insofar as these rejections may be applied against the amended claims, they should be deemed overcome.

Claim 1 has been amended to more particularly describe a distinguishing feature of the present invention. The charge leakage correction circuit is configured to: "measure a first voltage across the Low Pass Filter (LPF) at lock; measure a second voltage across the LPF periodically after lock; add charge to the LPF if the rate of change of voltage across the LPF is negative; and subtract charge from the LPF if the rate of change is positive." Support for this amendment can be found, among other places, at page 8, lines 2-23 of the original Application.

The Nakao reference does not teach, suggest, or disclose this feature of the present invention. Specifically, Nakao discloses an apparatus to remove in-phase noise in a Phase Lock Loop (PLL) by comparing two signals from the LPF. Alternatively, the present invention uses a charge leakage correction circuit to stabilize the voltage of the LPF. The voltage of the LPF controls the frequency that is produced by the PLL, and a capacitor stores the voltage (charge) of the

LPF. Therefore, when the voltage across the LPF is too high the charge leakage correction circuit removes charge from the capacitor, and when the voltage across the LPF is too low the charge leakage correction circuit adds charge to the capacitor. The present invention determines whether to add or subtract charge by measuring the voltage difference between a measured voltage at lock and a measured voltage periodically after lock. This feature of the present invention is clearly not disclosed in the Nakao reference.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach, or suggest the unique combination now recited in amended Claim 1. Applicants therefore submit that amended Claim 1 is both clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable. Accordingly, Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 102(b) in view of Nakao be withdrawn and that amended Claim 1 be allowed.

Claim 2 depends upon and further limits amended Claim 1. Hence, for at least the aforementioned reasons, this Claim should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejection of dependent Claim 2 also be withdrawn.

Claim 3 has been amended to more particularly describe a distinguishing feature of the present invention. The differentiator of Claim 3 is configured to: "measure the rate of change of the voltage across the LPF by measuring a first voltage at lock and a second voltage periodically after lock." In addition, the charge pump of Claim 3 is configured to: "add charge to the LPF if the rate of change is negative, and ... subtract charge from the LPF if the rate of change is positive." Support for this amendment can be found, among other places, at page 8, lines 2-23 of the original Application.

The Nakao reference does not teach, suggest, or disclose this feature of the present invention. Specifically, Nakao discloses an apparatus to remove in-phase noise in a Phase Lock Loop (PLL) by comparing two signals from the LPF. Alternatively, the present invention uses a differentiator and a charge pump to stabilize the voltage of the LPF. Accordingly, when the voltage across the LPF is too high the charge pump removes charge from the capacitor, and when the voltage across the LPF is too low the charge pump adds charge to the capacitor. The differentiator determines whether to add or subtract charge by measuring the voltage difference between a measured voltage at lock and a measured voltage periodically after lock. This feature of the present invention is clearly not disclosed in the Nakao reference.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach, or suggest the unique combination now recited in amended Claim 3. Applicants therefore submit that amended Claim 3 is both clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable. Accordingly, Applicants respectfully request that the rejection of Claim 3 under 35 U.S.C. § 102(b) in view of Nakao be withdrawn and that amended Claim 3 be allowed.

Claim 4 depends upon and further limits amended Claim 3. Hence, for at least the aforementioned reasons, this Claim should be deemed to be in condition for allowance. Accordingly, Applicants respectfully request that the rejection of dependent Claim 4 also be withdrawn.

Claim 5 has been amended to more particularly describe a distinguishing feature of the present invention. The differentiator of Claim 5 is configured to: "measure the rate of change of the voltage across the LPF by measuring a first voltage at lock and a second voltage periodically after lock." In addition, the charge pump of Claim 5 is configured to: "add charge to the LPF if the rate

of change is negative, and ... subtract charge from the LPF if the rate of change is positive." Support for this amendment can be found, among other places, at page 8, lines 2-23 of the original Application.

The Nakao reference does not teach, suggest, or disclose this feature of the present invention. Specifically, Nakao discloses an apparatus to remove in-phase noise in a Phase Lock Loop (PLL) by comparing two signals from the LPF. Alternatively, the present invention uses a differentiator and a charge pump to stabilize the voltage of the LPF. Accordingly, when the voltage across the LPF is too high the charge pump removes charge from the capacitor, and when the voltage across the LPF is too low the charge pump adds charge to the capacitor. The differentiator determines whether to add or subtract charge by measuring the voltage difference between a measured voltage at lock and a measured voltage periodically after lock. This feature of the present invention is clearly not disclosed in the Nakao reference.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach, or suggest the unique combination now recited in amended Claim 5. Applicants therefore submit that amended Claim 5 is both clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable. Accordingly, Applicants respectfully request that the rejection of Claim 5 under 35 U.S.C. § 102(b) in view of Nakao be withdrawn and that amended Claim 5 be allowed.

Claim 6 has been amended to more particularly describe a distinguishing feature of the present invention. The limitation "measuring the rate of change for voltage across the LPF by measuring a first voltage at lock and a second voltage periodically after lock" has been added to Claim 6. Support for this amendment can be found, among other places, at page 8, lines 2-23 of the original Application.

The Nakao reference does not teach, suggest, or disclose this feature of the present invention. Specifically, Nakao discloses an apparatus to remove in-phase noise in a Phase Lock Loop (PLL) by comparing two signals from the LPF. Alternatively, the present invention measures two voltages across the LPF, and adds or removes charge from LPF to stabilize the voltage. Accordingly, when the voltage across the LPF is too high, charge is removed from the capacitor, and when the voltage across the LPF is too low, charge is added to the capacitor. The present invention determines whether to add or subtract charge by measuring the voltage difference between a measured voltage at lock and a measured voltage periodically after lock. This feature of the present invention is clearly not disclosed in the Nakao reference.

In view of the foregoing, it is apparent that the cited reference does not disclose, teach, or suggest the unique combination now recited in amended Claim 6. Applicants therefore submit that amended Claim 6 is both clearly and precisely distinguishable over the cited reference in a patentable sense, and is therefore allowable. Accordingly, Applicants respectfully request that the rejection of Claim 6 under 35 U.S.C. § 102(b) in view of Nakao be withdrawn and that amended Claim 6 be allowed.

Claim 8 stands rejected under 35 U.S.C. § 103(a) in view of Nakao, and U.S. Patent 5,663,890 to Saleh et al. ("Saleh"). Insofar as this rejection may be applied against the amended claims, it should be deemed overcome.

Claim 8 has been amended to more particularly describe a distinguishing feature of the present invention. The limitation "computer code for measuring the rate of change for voltage across the LPF by measuring a first voltage at lock and a second voltage periodically after lock" has been added to Claim 8. Support for this amendment can be found, among other places, at page 8, lines 2-23 of the original Application.

The Nakao and Saleh references do not teach, suggest, or disclose this feature of the present invention. Specifically, Nakao discloses an apparatus to remove in-phase noise in a Phase Lock Loop (PLL) by comparing two signals from the LPF, and Saleh discloses an apparatus comprising a circuit to be executed by a computer program product. Alternatively, the present invention claims a computer program product that measures two voltages across the LPF, and adds or removes charge from LPF to stabilize the voltage. Accordingly, when the voltage across the LPF is too high, charge is removed from the capacitor, and when the voltage across the LPF is too low, charge is added to the capacitor. The present invention uses computer code to determine whether to add or subtract charge by measuring the voltage difference between a measured voltage at lock and a measured voltage periodically after lock. This feature of the present invention is clearly not disclosed in the Nakao and Saleh references, taken either singularly or in combination.

In view of the foregoing, it is apparent that the cited references do not disclose, teach, or suggest the unique combination now recited in amended Claim 8. Applicants therefore submit that amended Claim 8 is both clearly and precisely distinguishable over the cited references in a patentable sense, and is therefore allowable. Accordingly, Applicants respectfully request that the rejection of Claim 8 under 35 U.S.C. § 102(b) in view of Nakao and Saleh be withdrawn and that amended Claim 8 be allowed.

In addition, the word "charge" replaces the word "voltage" in Claims 3 and 5. The word "negative" replaces the word "positive" in Claims 7 and 9. Furthermore, Claims 10-17 are new claims. Support for these new claims can be found, among other places, page 5, lines 9-14 of the original Application.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-17.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

Dated: 4/11/05

CARR LLP
670 Founders Square
900 Jackson Street
Dallas, Texas 75202
Telephone: (214) 760-3030
Fax: (214) 760-3003

Gregory W. Carr
Reg. No. 31,093